A Distributed Optical Receiver Preamplifier with Unequal Gate/Drain Impedances

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Abstract

A near dc to 16.4 GHz wide band distributed amplifier, constructed using a 20 GHz MMIC GaAs process and optimised to operate as an optical receiver front end preamplifier, has been designed, realised and tested at 10 Gbit/s. The design uses a 75Ω gate line impedance to maximise the overall transimpedance gain without introducing severe bandwidth restriction.

Introduction

Distributed amplifier MMIC structures are attractive for use as preamplifiers for optical receiver applications operating in the multi Gbit/s region. Traditionally, such amplifiers have been designed in a similar way to distributed amplifiers intended for use in microwave applications where equal gate and drain line characteristic impedances are typically set to 50Ω to match the input source and output load impedances, respectively [1,2]. For optical receivers the effective transimpedance gain, defined as the ratio of the output voltage signal to the input photocurrent, is given as the product of the amplifier's input impedance and voltage gain. Since the input to an optical receiver preamplifier is provided by a photodiode, a predominantly capacitive current source, receiver gain can be maximised by increasing the input load resistance at the expense of compromising the bandwidth [3]. Therefore, if a distributed amplifier is to be used as a receiver preamplifier, with the photodiode directly connected to the input artificial transmission line, increased gain can be obtained if the gate line impedance and termination are increased beyond the standard 50Ω value. This can be done while keeping the drain line impedance fixed to 50Ω to match the following stage and applying phase compensation techniques [4,5] to ensure response flatness. Furthermore, increased gate line impedance leads to reduced input noise resulting in improved receiver sensitivity.

Impedance Ratio Limitations

Two factors limit the maximum gate line impedance to be used in a distributed amplifier optical receiver. The first factor, the input time constant, can be minimised by selecting a low capacitance photodiode. The second factor, though, relates to the finite cut-off frequency of the gate line and defines a maximum allowable gate to drain line impedance ratio for a given upper frequency or bit rate specification. For an ideal artificial transmission line constructed using ideal inductors and capacitances the gate line cutoff frequency is given by:

$$f_{c_g} = \frac{1}{\pi Z_g C_{gs}} \qquad (1)$$

where C_{gs} is the gate to source capacitance and Z_g is the characteristic impedance of the gate line. However, for practical MMIC implementation, where inductors are replaced by microstrip lines, this cutoff frequency is reduced. For the MESFETS used in our application, the cutoff frequency of the gate line versus the impedance ratio κ is plotted in Fig. 1, contrasted with the cutoff frequency of an ideal LC_{gs} gate line. In order to achieve flat frequency response and minimise group delay distortion, the κ factor is chosen to correspond to a gate cut-off frequency greater than 1.5 times the required 3dB point of the amplifier.

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Practical Design

The GMMT F20 GaAs process was used to implement a distributed amplifier suitable for operation at 10 Gbit/s and beyond. Six $2 \times 50\mu m$ MESFETs biased at I_{dss} were used and a microstrip line was inserted in series with each MESFET drain line to equalise the phase velocity between the input and output transmission lines. The $2 \times 50\mu m$ MESFET was chosen because it offers the smallest value of C_{gs} of all the standard MESFET cells. For operation up to 15 GHz to be possible κ is chosen to be 1.5 corresponding to a gate line cut-off frequency of 20 GHz (see Fig. 1), this allowed the gate line characteristic impedance to be set to 75Ω without compromising the transimpedance gain flatness and bandwidth. The small loss introduced by this device (MESFET) permitted six devices to be employed to obtain a transimpedance gain of 42.3 dBΩ. The PIN and the PIN/MMIC transition were modelled by the equivalent circuit represented in Fig. 2. The fabricated receiver microphotograph is shown in Fig. 3; its dimensions are 3mm×2mm. In the design, transmission line discontinuities were minimised by using curved lines instead of sharp corners and the coupling between lines was minimised by maintaining the transmission lines as far apart as possible within the layout constraints. Also, no on-chip capacitors are used for decoupling. This was done to avoid possible resonance of the bond-wire inductance with the capacitors and to allow the decoupling to be optimised off chip. Finally, the drain load (50 Ω) was split into eight 25 Ω resistors — two parallel arrangements of four resistors in series. With this arrangement it was possible to bias the receiver through the drain termination while maintaining linear behaviour of the load resistor. This scheme also permits the receiver to achieve DC operation. Fig. 4 shows the simulated transimpedance and group delay frequency behaviour of the distributed receiver, which exhibits a 3 dB bandwidth of 16.4 GHz, a transimpedance gain of 42.2 ± 1.4 dBΩ and a group delay of 110 ± 40 ps within the pass-band. It should be noted that the overall frequency response of the transimpedance gain is sensitive to the photodidode capacitance C_d. Finally, Fig. 5 shows the simulated eye-diagrams for 10 and 20 Gbit/s operation.

Results and Experimental Testing

The distributed amplifier was fully packaged with a PIN photodiode chip. The gain, frequency and delay responses were tested using an optical network analyzer while testing with digital data sequences was carried on an optical fiber 10 Gbit/s test-bed. Fig. 6 shows the measured transimpedance in dB (normalised to 50Ω) and the group delay in ps, both measured up to 20 GHz. The experimental receiver also exhibits a 16.4 GHz 3 dB bandwidth. The discrepancy between the simulated and the experimental transimpedance gain is within ±1.5 dB for the frequency range 0.13-12 GHz. For 10 Gbit/s 2^7-1 PRBS NRZ data, the received bit pattern at the output of the distributed amplifier as well as the transmitted bit pattern are shown in Fig. 7, demonstrating practical operation at 10 Gbit/s. From the receiver measurements, operation beyond 10 Gbit/s is expected to be practical at the expense of increased intersymbol interference and the consequent error rate degradation.

Conclusion

The design, simulation and experimental results of a 16.4 GHz wide band distributed optical receiver with a transimpedance gain of approximately 42.2 dBΩ have been presented. This distributed optical receiver uses unequal drain/gate characteristic impedances to achieve low noise, high transimpedance and wide band operation, appropriate for bit rates well over 10 Gbit/s.

References

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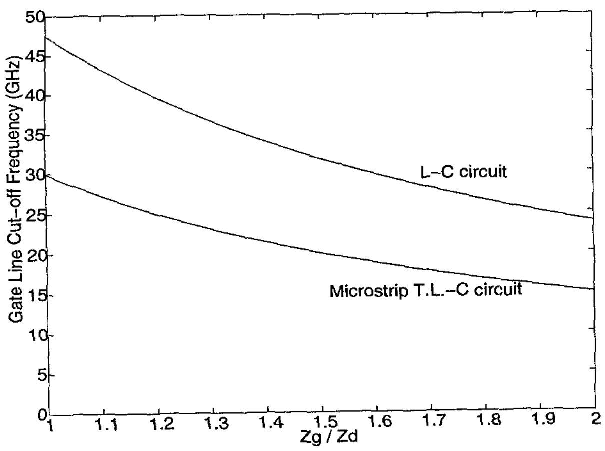

Figure 1: **Gate Cut-off Frequency versus** κ

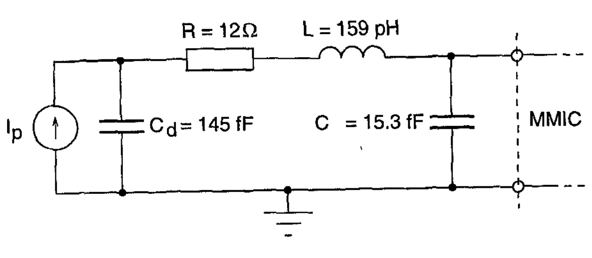

Figure 2: **PIN and PIN/MMIC transition equivalent circuit**

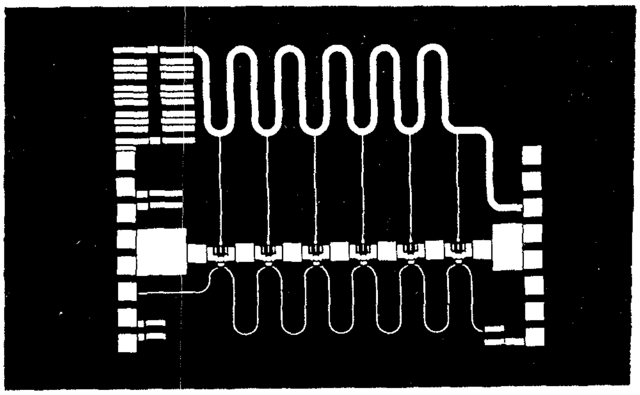

Figure 3: **Photomicrograph of the Distributed Amplifier**

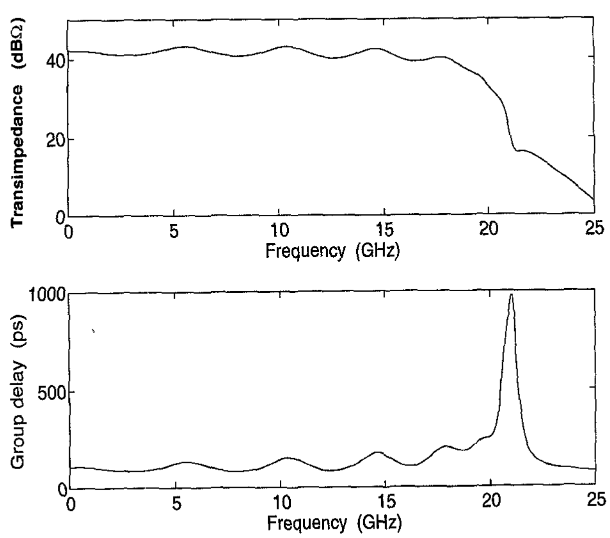

Figure 4: **Distributed Receiver Transimpedance and Group Delay**

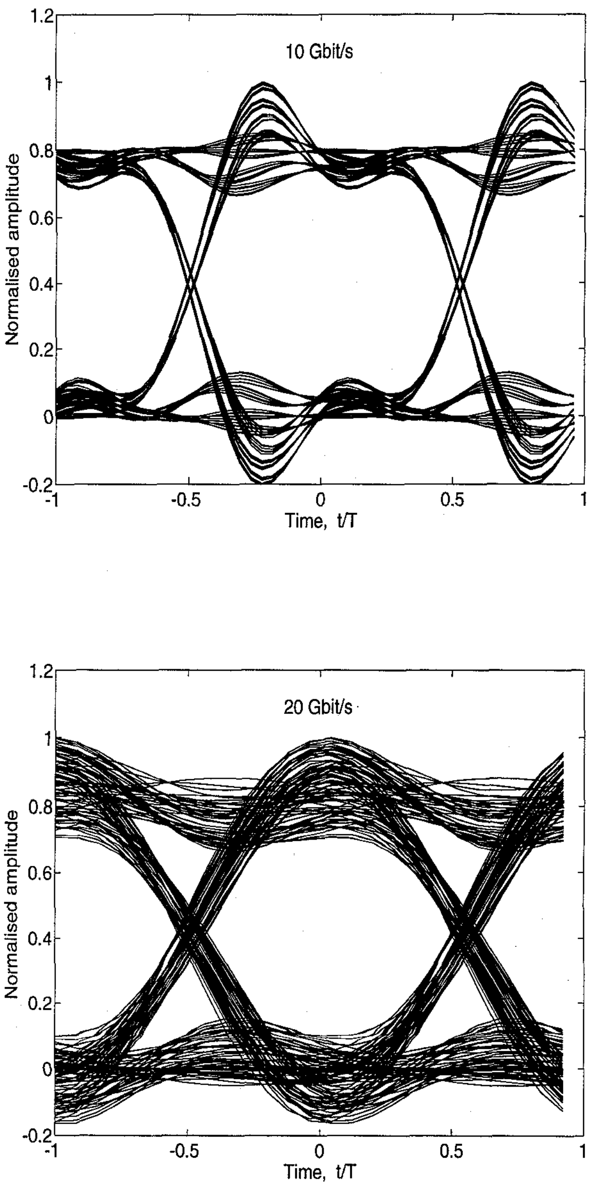

Figure 5: **Eye-diagrams**

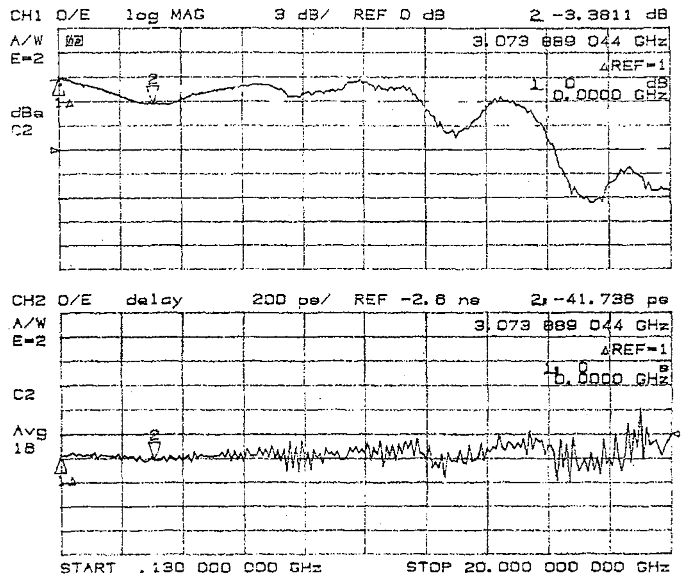

Figure 6: **Experimental Transimpedance Gain and Group Delay**

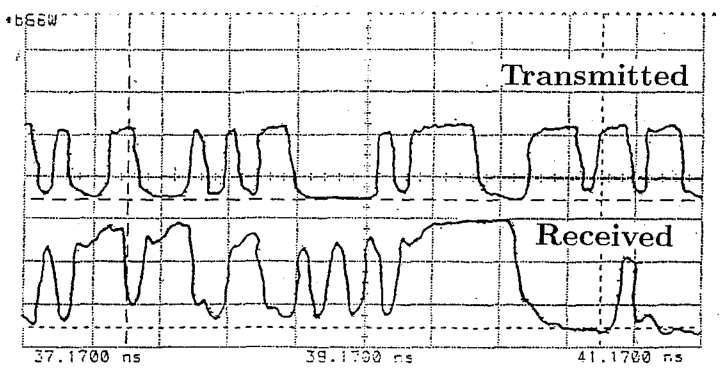

Figure 7: **Transmitted and Received Bit Pattern**